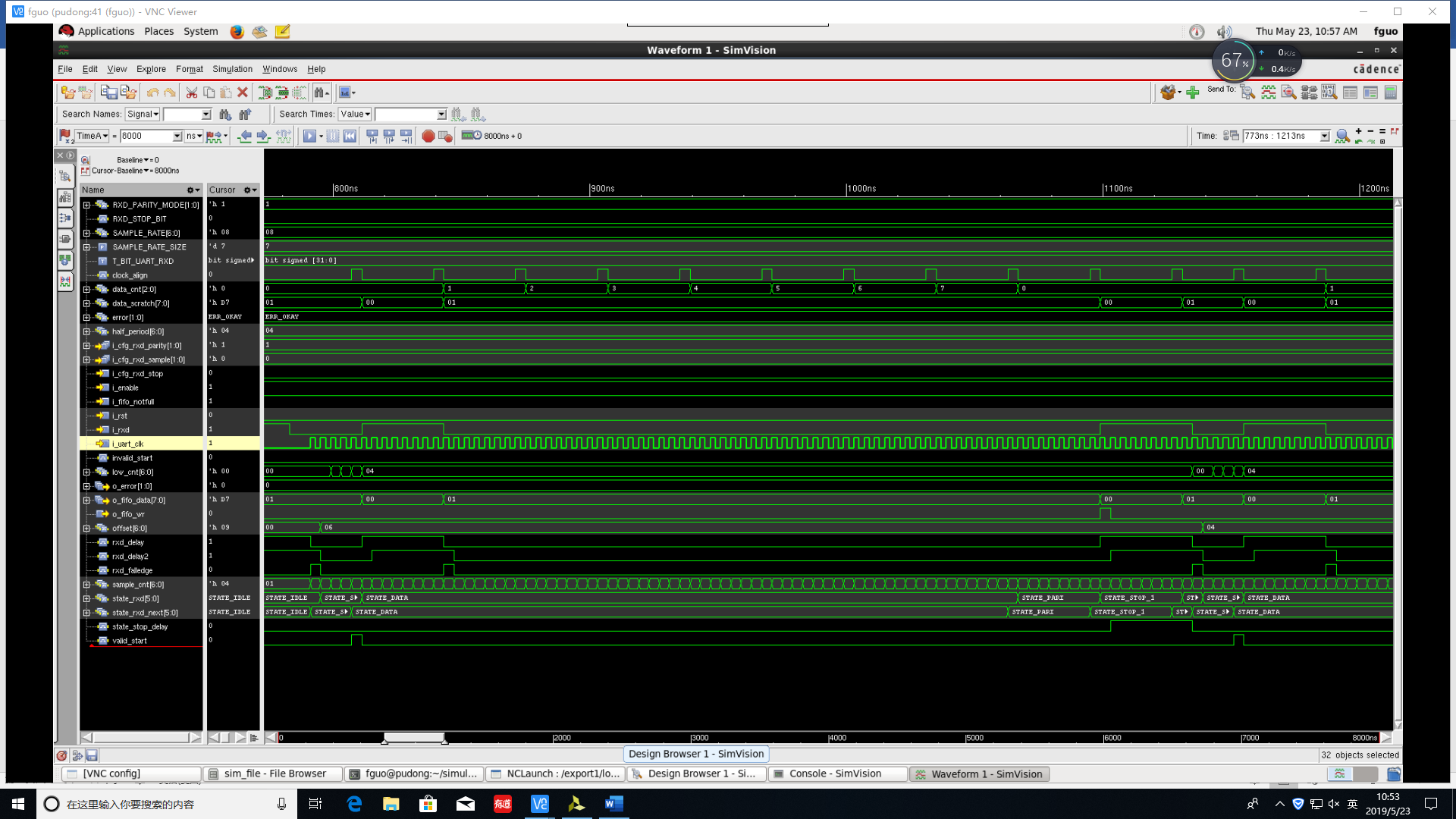
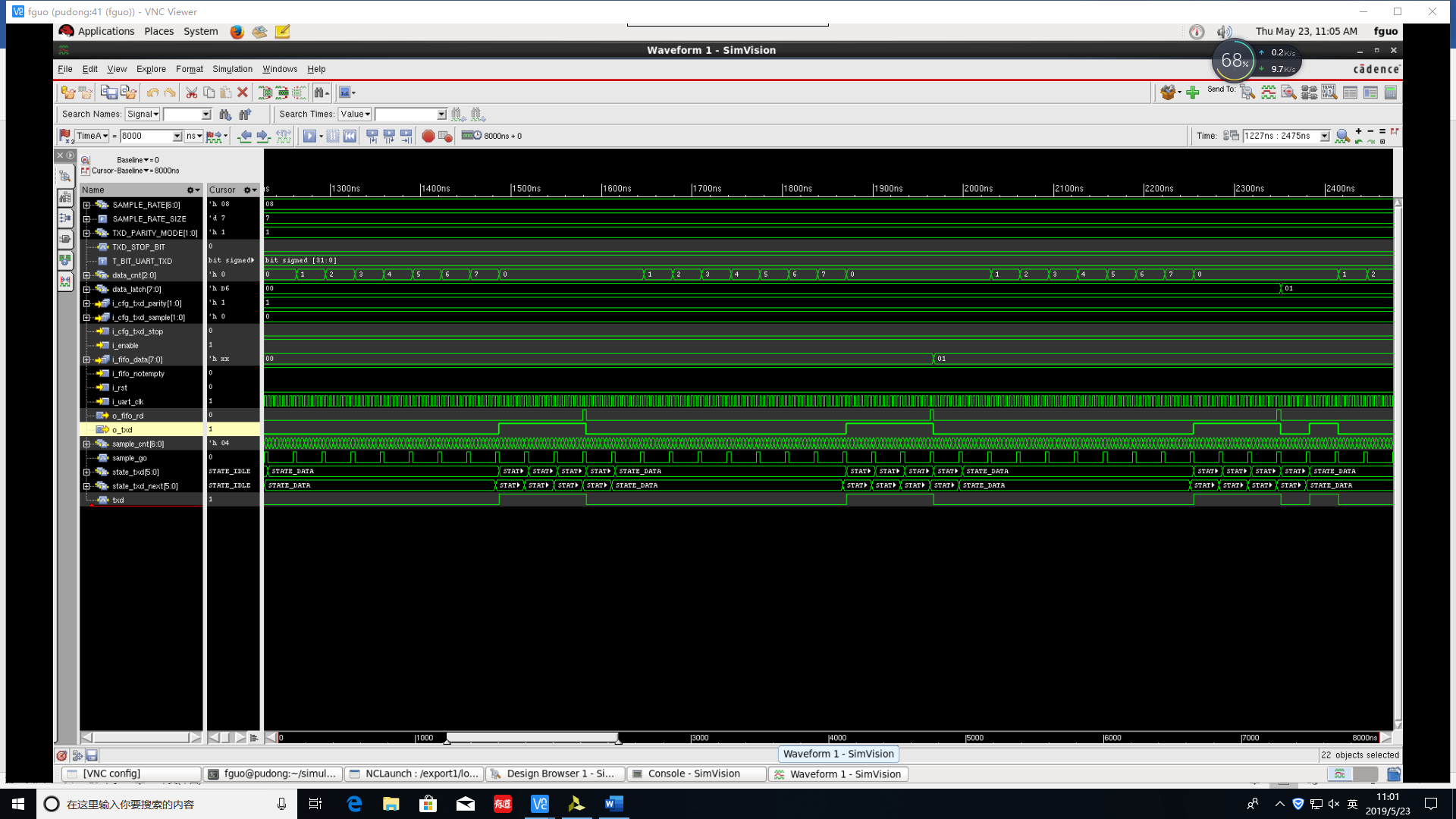
1. This week, I mainly do the verification of the uart protocol as a whole.



This is the simulation of rxd.



This is the simulation of txd.

The test file is in the server of Lab.

2. I learn the class of the SystemVerilog.

3. I write several Verilog module.